AMENDMENTS TO THE CLAIMS

1. (previously presented) A method for reducing shallow trench isolation (STI) consumption during semiconductor device processing, the method comprising:

forming a hardmask over a semiconductor substrate;

patterning said hardmask and forming a trench within said substrate;

filling said trench with an insulative material;

implanting said insulative material with boron ions with remaining portions of said hardmask still in place so as to prevent said boron ions from being implanted within active areas of said semiconductor substrate; and

annealing said insulative material.

2. (original) The method of claim 1, wherein said hardmask further comprises:

a pad oxide material formed on said substrate; and

a pad nitride material formed on said pad oxide.

3. (original) The method of claim 1, further comprising recessing a portion of said insulative material prior to said implanting said insulative material.

4. (original) The method of claim 1, wherein said implanting said insulative material is carried out at a boron ion dose of about 1×10^{15} atoms/cm^2 to about 2×10^{16} atoms/cm^2.

5. (original) The method of claim 1, wherein said implanting said insulative material is carried out at a boron ion dose of about 3×10^{15} atoms/cm^2 to about 1×10^{16} atoms/cm^2.

6. (original) The method of claim 1, wherein said implanting said insulative material is carried out at a boron ion dose of about 6×10^{15} atoms/cm^2.

7. (original) The method of claim 1, further comprising forming a nitride liner within said trench prior to said filling said trench with an insulative material.

8. (original) The method of claim 1, further comprising forming a thermal oxide liner within said trench prior to said filling said trench with an insulative material.

9. (original) The method of claim 1, wherein said insulative material further comprises a high-density plasma oxide (HDP) material.

10. (previously presented) A semiconductor device trench isolation structure, comprising:

a substrate having a trench region filled with an insulative material, wherein said insulative material is implanted with boron ions and thereafter annealed, said boron ions implanted with a patterned hardmask protecting active areas of a semiconductor substrate so as to prevent said boron ions from being implanted within said active areas of said semiconductor substrate, thereby self-aligning said boron ions to said trench region.

11. (cancelled)

12. (original) The trench isolation structure of claim 10, wherein said boron ions are implanted at a dose of about 1×10^{15} atoms/cm^2 to about 2×10^{16} atoms/cm^2.

13. (original) The trench isolation structure of claim 10, wherein said boron ions are implanted at a dose of about 3×10^{15} atoms/cm^2 to about 1×10^{16} atoms/cm^2.

14. (original) The trench isolation structure of claim 10, wherein said boron ions are implanted at a dose of about 6×10^{15} atoms/cm^2.

15. (original) The trench isolation structure of claim 10, wherein said insulative material is formed over a nitride liner formed within said trench.

16. (original) The trench isolation structure of claim 10, wherein said insulative material is formed over a thermal oxide liner formed within said trench.

17. (original) The trench isolation structure of claim 10, wherein said insulative material further comprises a high-density plasma oxide (HDP) material.

18-23. (cancelled)